UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,365	08/15/2001	Masahiro Takeuchi	15.45/6059	3437

24033 7590 02/17/2004

KONRAD RAYNES & VICTOR, LLP
315 S. BEVERLY DRIVE
210
BEVERLY HILLS, CA 90212

EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,365	TAKEUCHI, MASAHIRO	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-26,32-56 and 60-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-26,32-56 and 60-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11/03/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,303,432 to Horita et al. and US Patent No. 6,548,373 to Chuang et al.

Regarding claim 20, Li et al. teach the first layer (112) comprises an epitaxial growth layer.

Regarding claim 21, Li et al. teach removing the polishing stopper layer (116) after planarizing the dielectric layer (122).

Regarding claim 22, Li et al. teach an oxidizing at least a portion of the first layer (112) in the at least one trench prior to forming the dielectric layer in and above the trench.

Regarding claim 23, Li et al. teach forming a pad layer (114) between the first layer (112) and the polishing stopper layer (116).

Regarding claim 24, Li et al. (figures 3a-m) teach a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor substrate (110) having a first layer (112);

forming a pad layer (114) on the first layer (112);

forming a polishing stopper layer (116) on the pad layer (114);

forming at least one trench by etching the first layer (112) while using at least the polishing stopper layer (116) as a mask;

forming a dielectric layer (122) in and above the trench;

planarizing the dielectric layer using the polishing stopper layer (116) as a stopper;

removing the polishing stopper layer (116) after planarizing the dielectric layer (122);

removing the pad layer (114) after the moving the polishing stopper layer (116);

forming a sacrificial oxide layer (136) on the first layer (112) after the removing the pad layer (114); and

implanting impurities to form a well in the first layer adjacent to the trench.

Li et al. differ from the claimed invention by not showing implanting impurities to form a well in the first layer adjacent to the trench after the thermally treating the dielectric layer. However, Horita et al. teach forming a well after the thermally treating the dielectric layer (column 9, lines 9-16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Horita et al. into the method taught by Li et al. because it eliminates the contamination and recovers the polishing defect. The combined device shows implanting impurities to form a well in the first layer adjacent to the trench after the thermally treating the dielectric layer.

Li et al. and Horita et al. differ from the claimed invention by not showing thermally treating the dielectric layer after the forming the sacrificial oxide layer. However, Chuang et al. (figures 1 a-c) teach thermally treating the dielectric layer after forming sacrificial oxide layer (column 3, lines 5-44). Therefore, it would have been obvious to one having ordinary skill in the

art at the time the invention was made to incorporate the teaching of Chuang et al. into the method taught by Li et al. and Horita et al. because it reduces the damage of silicon layer. The combined device shows thermally treating the dielectric layer after the forming the sacrificial oxide layer.

Li et al., Horita et al. and Chuang et al. further differ from the claimed invention by not showing thermally treating the dielectric layer at a temperature of at least about 1050° C after the forming the sacrificial oxide layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for thermally treating the dielectric layer to a thermal treatment at a temperature of at least 1050° C because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 25, Li et al., Horita et al. and Chuang et al. differ from the claimed invention by not showing the thermally treating the dielectric layer is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the thermally treating the dielectric layer is carried out in an atmosphere comprising 0.1 volume % to 10 volume % oxygen because it is densified the dielectric layer. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

3. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Horita et al. in view of Chuang et al., and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 26, the disclosures of Li et al., Horita et al. and Chuang et al. are discussed as applied to claims 20-25 above.

Li et al., Horita et al. and Chuang et al. differ from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the method taught by Li et al., Horita et al. and Chuang et al. because it improves the dielectric property of the dielectric layer.

4. Claims 32-34, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,303,432 to Horita et al. and US Patent No. 6,028,339 to Frenette et al.

Regarding claim 32, Li et al. (figures 3a-m) teach a method for manufacturing a semiconductor device, comprising:

providing a semiconductor layer (112);

forming a plurality of trenches in the semiconductor layer (112);

forming a thermal oxide layer (120) on the semiconductor surface in the trenches; and

depositing a dielectric layer (122) into the trenches and filling the trenches with the dielectric layer (122).

Li et al. differ from the claimed invention by not showing the thermally treating the dielectric layer in the trenches at a temperature about 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally treating the dielectric layer in the trenches at a temperature about 1050° C because it is densified the dielectric layer, eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Li et al. differ from the claimed invention by not showing implanting impurities to form a well after the thermally treating the dielectric layer. However, Horita et al. teach forming a well after the thermally treating the dielectric layer (column 9, lines 9-16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Horita et al. into the method taught by Li et al. because it eliminates the contamination and recovers the polishing defect. The combined device shows implanting impurities to form a well after the thermally treating the dielectric layer.

Li et al. and Horita et al. further differ form the claimed invention by not showing forming a well region between a first trench and a second trench of the plurality of trenches, wherein the first trench is adjacent to the second trench, and wherein the well region is formed to extend continuously in the semiconductor layer from the first trench to the second trench. However, Frenette et al. (figure 1) teach forming a well region between a first trench and a second trench of the plurality of trenches, wherein the first trench is adjacent to the second trench, and wherein the well region is formed to extend continuously in the semiconductor layer from the first trench to the second trench. It would have been obvious to one having ordinary skill in the art at the time

the invention was made to incorporate the teaching of Frenette et al. into the device taught by Li et al. and Horita et al. since it is a well known method.

Regarding claim 33, the combined device shows the dielectric layer (Li et al.; 122) is formed in direct contact with the thermal oxide layer (Li et al.; 120) in the trenches (Li et al.; 118a, 118b).

Regarding claim 34, Li et al., Horita et al. and Frenette et al. differ from the claimed invention by not showing the dielectric layer is formed with a film density of at lest 2.1 g/cm^3. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at least 2.1 g/cm^3 because it provides a good gap-fill characteristic. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 38, the combined device shows forming a polishing stopper layer (Li et al.; 116) on the semiconductor layer (Li et al.; 112) prior to form the plurality of trenches (Li et al.; 118a, 118b);

forming openings in the polishing stopper layer (Li et al.; 116) above the regions in the semiconductor layer where the plurality of trenches are to be formed;

forming the dielectric layer (Li et al.; 122) in the openings and on the polishing stopper layer;

planarizing the dielectric layer using the polishing stopper layer as a stop; and

removing the polishing stopper layer after planarizing the dielectric layer and prior to the thermally treating the dielectric layer (Horita et al.).

Regarding claim 39, the combined device shows forming an oxide pad layer (Li et al.; 114) on the semiconductor layer (Li et al.; 112) prior to form the polishing stopper layer (Li et al.; 116).

5. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. and Horita et al. in view of Frenette et al., and further in view of US Patent No. 6,165,854 to Wu.

The disclosures of Li et al., Horita et al. and Frenette et al. are discussed as applied to claims 32-34, 38 and 39 above.

Regarding claim 35, Li et al., Horita et al. and Frenette et al. differ from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the method taught by Li et al., Horita et al. and Frenette et al. because it improves the dielectric property of the dielectric layer.

Regarding claim 36, the combined device shows the semiconductor layer (Li et al.; 112) comprises an epitaxial growth layer formed on a semiconductor substrate (Li et al.; 110).

Regarding claim 37, Li et al., Horita et al., Frenette et al. and Wu differ form the claimed invention by not showing the epitaxial growth layer has a thickness of at least 2 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the epitaxial growth layer has a thickness of at least 2 micrometer because it grows over ion implantation, so that the thickness of the doped layer may be readily controlled.

Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

6. Claims 40-49, 51-56, 60, 61 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,064,105 to Li et al. in view of US Patent No. 6,087,243 to Wang.

Regarding claim 40, Li et al. (figures 3a-m) teach a method for manufacturing a semiconductor device having a trench isolation region, the method comprising:

forming a polishing stopper layer (116) on a semiconductor layer (112);

forming an opening in the polishing stopper layer (116) and a trench in the semiconductor layer (110);

forming a dielectric layer (122) in the trench, in the opening in the stopper layer (116), and on the stopper layer;

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper; and

removing the polishing stopper layer (116) after the planarizing the dielectric layer (122);

Li et al. differ from the claimed invention by not showing conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer. However, Wang teaches conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer (column 6, lines 44-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wang into the method taught by Li et al. because it is densified the dielectric layer, eliminates the contamination and

recovers the polishing defect. The combined device shows conducting a thermal treatment of the dielectric layer after removing the polishing stopper layer and forming a well in the semiconductor layer after the thermal treatment of the dielectric layer.

Li et al. and Wang differ from the claimed invention by not showing the thermal treatment is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment is conducted at a temperature of at least 1050° C because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 41, the combined device shows forming a pad layer (Li et al.; 114) on the semiconductor layer (Li et al.; 112) prior to form the polishing stopper layer (Li et al.; 116), wherein the pad layer is formed between and in direct contact with the semiconductor layer and the polishing stopper layer.

Regarding claim 42, the combined device shows the opening in the polishing stopper layer (Li et al.; 116) also extends through the pad layer (Li et al.; 114).

Regarding claim 43, Li et al. and Wang differ from the claimed invention by not showing isotropically etching the pad layer and upper portions of the dielectric layer after the removing the polishing stopper layer and prior to the conducting the thermal treatment. It would have been obvious to one having ordinary skill in the art at the time the invention was made for isotropically etching the pad layer and the dielectric layer because it proceeds in all directions at the same rate.

Regarding claim 44, the disclosures of Li et al. and Wang are discussed as applied to claim 43 above. The combined device further shows etching exposes upper surfaces of the semiconductor layer (Li et al.; 112).

Regarding claim 45, the disclosures of Li et al. and Wang are discussed as applied to claims 43-44 above. The combined device further shows an oxide layer (Li et al.; 122) is formed on the exposed upper surfaces of the semiconductor layer (Li et al.; 112) after the etching and prior to the forming a well in the semiconductor layer.

Regarding claim 46, the combined device shows the oxide layer (Li et al.; 122) is formed prior to the conducting a thermal treatment of the dielectric layer.

Regarding claim 47, Li et al. and Wang differ from the claimed invention by not showing the dielectric layer is formed with a film density of at lest 2.1 g/cm^3. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dielectric layer is formed with a film density of at least 2.1 g/cm^3 because it provides a good gap-fill characteristic. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 48, Li et al. and Wang differ from the claimed invention by not showing the temperature of the thermal treatment is 1100° C or higher. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the temperature of the thermal treatment is 1100° C or higher because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are

disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 49, Li et al. and Wang differs from the claimed invention by not showing the temperature of the thermal treatment is in the range 1050° C to 1250° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the temperature of the thermal treatment is in the range 1050° C to 1250° C because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 51, the combined device shows the trench includes sidewall surfaces and a bottom surface, the method further comprising of thermally oxidizing the sidewall surfaces and the bottom surface of the trench to form a thermal oxide layer (Li et al.; 120) thereon, wherein the dielectric layer (Li et al.; 122) is formed in direct contact with the thermal oxide layer (Li et al.; 120).

Regarding claim 52, Li et al. and Wang differ from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700° C to 1150° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall surfaces and the bottom surface of the trench is carried out at a temperature in the range of at 700° C to 1150° C because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the

prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 53, the disclosures of Li et al. and Wang are discussed as applied to claim 52.

Regarding claim 54, Li et al. and Wang differ from the claimed invention by not showing the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermally oxidizing the sidewall surfaces and the bottom surface yields an oxidation layer having a thickness in the range of 10 nm to 100 nm because it protects the damages on the surface of substrate. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 55, the combined device shows the semiconductor layer (Li et al.; 112) comprises an epitaxial growth layer formed on a semiconductor substrate (Li et al.; 110).

Regarding claim 56, Li et al. and Wang differ from the claimed invention by not showing the trench is formed with a trench width of no greater than 0.35 micrometer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the trench is formed with a trench width of no greater than 0.35 micrometer because it reduces the thickness of the device. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 60, Li et al. (figures 3a-m) teaches a method for manufacturing a semiconductor device including a trench isolation region, the method comprising:

providing a semiconductor layer (112);

forming a pad oxide layer (114) on the semiconductor layer (112);

forming a polishing stopper layer (116) in direct contact with the pad oxide layer (114), wherein the pad oxide layer (114) is positioned between the semiconductor layer (112) and the polishing spotter layer (116);

forming a patterned resist layer on the polishing stopper layer (116), the patterned resist layer including an open region exposing part of the polishing stopper layer (116) over a trench formation region;

using the patterned resist layer as a mask, etching the polishing stopper layer (116) and the pad oxide layer (114) so that a portion of the semiconductor layer (112) is exposed;

after the etching removing the patterned resist layer;

after the removing the patterned resist layer, etching the semiconductor layer (112) to form at least one trench therein, using the polishing stopper layer (116) as a mask;

forming a dielectric layer (122) in and above the at least one trench;

planarizing the dielectric layer (122) using the polishing stopper layer (116) as a stopper; and

removing the polishing stopper layer (116) and the pad oxide layer (114).

Li et al. differ from the claimed invention by not showing heating the dielectric layer. However, Wang teaches heating the dielectric layer (column 6, lines 44-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

incorporate the teaching of Wang into the method taught by Li et al. because it is densified the dielectric layer, eliminates the contamination and recovers the polishing defect. The combined device shows heating the dielectric layer.

Li et al. and Wang differ from the claimed invention by not showing the thermal treatment is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment is conducted at a temperature of at least 1050° C because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 61, the combined device shows after forming the at least one trench and prior to form the dielectric layer (Li et al.; 122), forming a thermal oxide layer (Li et al.; 120) on the semiconductor substrate (Li et al.; 110) in the at least one trench.

Regarding claim 62, Li et al. and Wang differ from the claimed invention by not showing the thermal treatment is conducted at a temperature of at least 1050° C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thermal treatment is conducted at a temperature of at least 1050° C because it eliminates the contamination and recovers the polishing defect. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in view of Wang, and further in view of US Patent No. 6,165,854 to Wu.

Regarding claim 50, the disclosures of Li et al. and Wang are discussed as applied to claims 40-49, 51-56, 60, 61 and 62 above.

Li et al. and Wang differ from the claimed invention by not showing the dielectric layer is formed using high density plasma chemical vapor deposition. However, Wu teaches the dielectric layer (14) is formed using high density plasma chemical vapor deposition (column 4, lines 28-31). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Wu into the method taught by Li et al. and Wang because it improves the dielectric property of the dielectric layer.

Response to Arguments

Applicant's arguments with respect to claim 20-26, 32-56 and 60-62 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
January 22, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800